REMARKS

Claims 32, 57, 59, 61, and 97 have been amended. Claims 32-55, 57-68 and 97 are pending. Applicants reserve the right to pursue the original claims and other claims in this and other applications. Applicants respectfully request reconsideration of the above-referenced application in light of the amendments and following remarks.

Claims 32-61, 64-68, and 97 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No.: 6,475,854 ("Narwankar"). The rejection is respectfully traversed.

The cited reference fails to teach the subject matter of amended independent claims 32 and 97. Specifically, Narwankar does not disclose a method of forming a capacitor comprising, *inter alia*, "forming a bottom conducting layer . . . forming a dielectric layer over the bottom conducting layer; forming a top electrode that consists of a single top conducting layer . . . and annealing the single top conducting layer . . . with an oxidizing gas anneal."

Similarly, Narwankar does not teach a method of forming a capacitor comprising, *inter alia*, "forming a bottom conducting layer . . . [which] is a bottom electrode; forming a dielectric layer over the bottom electrode; forming a top electrode . . . comprising a bottom and a top conducting layer; and annealing said top conducting layer of said top electrode with an oxidizing gas anneal."

The Office Action asserts that Narwankar discloses a method of forming a capacitor with a bottom conducting layer 909, 602, 604, 605, a dielectric layer 912, 606, and a top conducting layer 608, 610, and annealing the entire top conducting layer. However, Narwankar also discloses that a "*second* upper metal layer 612 is then deposited *onto* the upper oxygen containing layer 610." (Col. 11, lines 16-17) (emphasis

added). The combination of "[t]he upper oxygen-containing layer 610 *and* the second upper metal layer 612 *together* form the *upper electrode 615* for the capacitor structure 650." (Col. 11, lines 33-36) (emphasis added).

In other words, Narwankar fails to disclose a method comprising, *inter alia*, of "forming a top electrode that consists of a single top conducting layer . . . and annealing the single top conducting layer . . . with an oxidizing gas anneal," as recited in claim 32, or a method comprising, *inter alia*, of "forming a top electrode . . . comprising a bottom and a top conducting layer; and annealing [the] top conducting layer of [the] top electrode with an oxidizing gas anneal.," as recited in claim 97. Narwankar top or upper electrode 615, comprises at least *two* layers: layers 610 and 612. The top layer 612 is *not* an oxidized gas annealed layer. Narwankar's layer 610 is formed *underneath* top layer 612. As such, Narwankar's top electrode 615 comprises at least two layers, and, the top layer 612 of the top electrode 615 does *not* undergo the oxidizing gas anneal.

Applicants' specification provides that "during subsequent wafer fabrication, the dielectric layer develops oxygen vacancies which contribute to capacitor current leakage." (Pg. 3, lines 20-22). Applicants' claimed capacitor "improves the dielectric property of the dielectric layer 36 by adding an oxidizing gas anneal (second anneal) which fills the oxygen voids created in the dielectric layer 36 after the top conducting layer 38 is deposited." (Applicants' specification, pg. 8, lines 8-10) (emphasis added).

Narwankar, in contrast, discloses that the second metal layer 612 is deposited *after* the first metal layer 608 is annealed (which becomes layer 610). Since Narwankar teaches that the top layer, here, metal layer 612, is deposited *after* the oxidizing anneal, oxygen voids would still be present in the dielectric layer. Consequently, Narwankar merely discloses forming a *conventional* top electrode, comprising two separate layers 610 and 612, and *not* Applicants' claimed method of a single layer for the electrode,

much less a top electrode comprising a bottom and a top layer, wherein the top layer undergoes an oxidizing gas anneal.

For at least these reasons, claims 32 and 97 should be allowable over Narwankar. Claims 32-61 and 64-68 depend from claim 32 and should be similarly allowable along with claim 32 for at least the reasons provided above, and on their own merits.

Claims 62 and 63 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Narwankar. The rejection is respectfully traversed.

Claims 62 and 63 depend from claim 32 and are similarly allowable along with claim 32 for at least the reasons provided above, and on their own merits. In particular, Narwankar fails to disclose a method comprising, *inter alia*, of "forming a top electrode that consists of a single top conducting layer . . . and annealing the single top conducting layer . . . with an oxidizing gas anneal," as recited in claim 32, or a method comprising, *inter alia*, of "forming a top electrode . . . comprising a bottom and a top conducting layer; and annealing [the] top conducting layer of [the] top electrode with an oxidizing gas anneal.," as recited in claim 97. As indicated above, Narwankar's top electrode 615 comprises at least two layers, and, the top layer 612 of the top electrode 615 does *not* undergo the oxidizing gas anneal.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to review and pass this application to issue.

Dated: June 13, 2005

Respectfully submitted,

By_____

Thomas J. D'Amico
Registration No.: 28,371
DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorney for Applicants